WHAT IS CLAIMED IS:

1. A method for transferring data in a system including a host computer system coupled through a communication medium to a data acquisition device, the method comprising:

configuring a data acquisition device for a data input/output (I/O) operation, wherein the data acquisition device comprises a link buffer;

the host computer preparing a plurality of transfer links, wherein each of the plurality of transfer links specifies a transfer of data between the data acquisition device and the host computer;

the host computer transferring the plurality of transfer links to a link buffer of the data acquisition device over the communication medium;

the data acquisition device initiating the data I/O operation; and

the data acquisition device executing the plurality of transfer links from the link buffer to transfer data between a data buffer in the data acquisition device and host memory in the host computer system;

2. The method of claim 1, wherein said host computer transferring the plurality of transfer links to a link buffer of the data acquisition device comprises the data acquisition device fetching the plurality of transfer links to the link buffer of the data acquisition device.

3. The method of claim 1, wherein the data acquisition device is operable to execute a first plurality of transfer links from a first portion of the link buffer while the host computer transfers a second plurality of transfer links over the communication medium to a second portion of the link buffer, thereby providing a double buffering mechanism for transferring the links from the host computer system to the link buffer in the data acquisition device.

4. The method of claim 3,

wherein the data acquisition device initiating the data I/O operation comprises the host computer initiating a data acquisition process on the data acquisition device;

wherein the data acquisition device comprises a DMA Controller, and

wherein the data acquisition device executing the plurality of transfer links from the link buffer comprises:

the data acquisition device acquiring data and storing the data in the data buffer;

the DMA Controller executing the plurality of links to transfer the data over the communication medium to the host memory in the host computer.

5. The method of claim 3,

wherein the host computer initiating the I/O operation on the data acquisition device comprises the host computer initiating a data generation operation on the data acquisition device;

wherein the data acquisition device comprises a DMA Controller, and

wherein the data acquisition device executing the plurality of transfer links from the memory buffer comprises:

the data acquisition device notifying the DMA Controller;

the data acquisition device requesting data from the DMA Controller; and

the DMA Controller executing the plurality of links to transfer the data from the memory of the host computer to the data buffer of the data acquisition device.

6. The method of claim 3, wherein the data acquisition device executing the plurality of transfer links from the link buffer comprises:

the host computer transferring a first plurality of transfer links to a first portion of the link buffer and a second plurality of transfer links to a second portion of the link buffer;

the data acquisition device executing the first plurality of transfer links from the first portion of the link buffer;

the host computer transferring a third plurality of transfer links to the first portion of the link buffer; and

the data acquisition device executing the second plurality of transfer links from the second portion of the link buffer.

7. The method of claim 6,

wherein the data acquisition device alternates between executing all transfer links from the first portion of the link buffer and all transfer links from the second portion of the link buffer, while the host computer alternates between transferring transfer links from the host computer to the second portion of the link buffer, and transferring transfer links from the host computer to the first portion of the link buffer, until there are no more transfer links to transfer from the host computer.

8. The method of claim 7,

wherein each link comprises at least one of a source address or a destination address, a count of a number of bytes in the transfer, and a pointer to a subsequent link.

9. The method of claim 7,

wherein one or more of the plurality of transfer links comprises a self configuration link, wherein the self configuration link comprises one or more instructions to move data to, from, or between the DMA Controller registers.

10. The method of claim 9,

wherein the self configuration link is inserted at the end of the first plurality of transfer links;

wherein, the DMA Controller executes the first plurality of transfer links on a DMA channel; and

wherein if the DMA channel reaches the self configuration link before the host computer has finished transferring the second plurality of transfer links to the second

portion of the link buffer, the self configuration link will stop the DMA channel to prevent data overruns.

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11. The method of claim 9,

wherein the self configuration link is inserted at the end of the second plurality of transfer links;

wherein, the DMA Controller executes the second plurality of transfer links on a DMA channel; and

wherein if the DMA channel reaches the self configuration link before the host computer has finished transferring the third plurality of transfer links to the first portion of the link buffer, the self configuration link will stop the DMA channel to prevent data overruns.

12. The method of claim 9,

wherein the self configuration link is inserted in the first plurality of transfer links;

wherein, the DMA Controller executes the first plurality of transfer links on a DMA channel; and

wherein when the DMA channel reaches the self configuration link the host is notified to begin transferring the second plurality of transfer links to the second portion of the link buffer.

13. The method of claim 9,

wherein the self configuration link is inserted in the second plurality of transfer links;

wherein, the DMA Controller executes the second plurality of transfer links on a DMA channel; and

wherein when the DMA channel reaches the self configuration link the host is notified to begin transferring the third plurality of transfer links to the first portion of the link buffer.

14. The method of claim 3,

wherein the communication medium comprises an IEEE 1394 bus, which is compliant with an IEEE 1394 protocol specification.

15. The method of claim 14,

wherein the data acquisition device comprises a PCI device,

wherein the data acquisition device further comprises a PCI/1394 translator;

the method further comprising the PCI/1394 translator translating messages between the IEEE 1394 protocol and PCI, thereby providing a mechanism for communication between the IEEE 1394 bus and the PCI device.

16. A system for transferring data over a communication medium, the system comprising:

a data acquisition device coupled to a first end of the communication medium, wherein the data acquisition device comprises a link buffer; and

a host computer system coupled to a second end of the communication medium, wherein the host computer system is operable to communicate through the communication medium to the data acquisition device;

wherein the host computer system is operable to prepare a plurality of transfer links and transfer the plurality of transfer links to the link buffer of the data acquisition device in a double buffered fashion, wherein each of the plurality of transfer links specifies a transfer of data between the data acquisition device and the host computer.

17. The method of claim 16, wherein said host computer being operable to transfer the plurality of transfer links to a link buffer of the data acquisition device comprises the data acquisition device being operable to fetch the plurality of transfer links to the link buffer of the data acquisition device.

18. The system of claim 16,

wherein the data acquisition device is operable to execute a first plurality of transfer links from a first portion of the link buffer while the host computer transfers a second plurality of transfer links from the host computer to a second portion of the link buffer, providing a double buffering mechanism for transferring data between the host computer system and the data acquisition device

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19. The system of claim 18,

wherein the host computer system is further operable to:

configure the data acquisition device for data input/output; and

initiate a data I/O operation on the data acquisition device, after the host computer system transfers the plurality of transfer links to the link buffer of the data acquisition device.

20. The method of claim 19,

wherein the host computer being operable to initiate the data I/O operation comprises the host computer being operable to initiate a data acquisition process on the data acquisition device;

wherein the data acquisition device comprises a DMA Controller, and

wherein the data acquisition device being operable to execute the plurality of transfer links from the link buffer comprises:

the data acquisition device being operable to acquire data and store the data in the data buffer; and

the DMA Controller being operable to execute the plurality of links to transfer the data over the communication medium to the host memory in the host computer.

21. The system of claim 19,

wherein the host computer being operable to initiate the I/O operation on the data acquisition device comprises the host computer being operable to initiate a data generation operation on the data acquisition device;

wherein the data acquisition device comprises a DMA Controller, and

wherein the data acquisition device being operable to execute the plurality of transfer links from the memory buffer comprises:

the data acquisition device being operable to notify the DMA Controller;

the data acquisition device being operable to request data from the DMA Controller; and

the DMA Controller being operable to execute the plurality of links to transfer the data from the memory of the host computer to the data buffer of the data acquisition device.

22. The system of claim 18, wherein the data acquisition device is operable to execute the plurality of transfer links from the link buffer;

wherein the data acquisition device being operable to execute the plurality of transfer links from the link buffer comprises:

the host computer being operable to transfer a first plurality of transfer links to a first portion of the link buffer and a second plurality of transfer links to a second portion of the link buffer;

the data acquisition device being operable to execute the first plurality of transfer links from the first portion of the link buffer;

the host computer being operable to transfer a third plurality of transfer links to the first portion of the link buffer; and

the data acquisition device being operable to execute the second plurality of transfer links from the second portion of the link buffer.

23. The system of claim 22,

wherein the data acquisition device is operable to alternate between executing all transfer links from the first portion of the link buffer and all transfer links from the second portion of the link buffer, while the host computer is operable to alternate between transferring transfer links from the host computer to the second portion of the

link buffer, and from the host computer to the first portion of the link buffer, until there are no more transfer links to transfer from the host computer.

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24. The system of claim 16,

wherein each link comprises at least one of a source address or a destination address, a count of a number of bytes in the transfer, and a pointer to a subsequent link.

25. The system of claim 16,

wherein one or more of the plurality of transfer links comprises a self configuration link, wherein the self configuration link comprises one or more instructions to move data to, from, or between the DMA Channel registers.

26. The system of claim 25,

wherein the self configuration link is inserted at the end of the first plurality of transfer links;

wherein, the DMA Controller executes the first plurality of transfer links on a DMA channel; and

wherein if the DMA channel reaches the self configuration link before the host computer has finished transferring the second plurality of transfer links to the second portion of the link buffer, the self configuration link will stop the DMA channel to prevent data overruns.

27. The system of claim 25,

wherein the self configuration link is inserted at the end of the second plurality of transfer links;

wherein, the DMA Controller executes the second plurality of transfer links on a DMA channel; and

wherein if the DMA channel reaches the self configuration link before the host computer has finished transferring the third plurality of transfer links to the first portion

of the link buffer, the self configuration link will stop the DMA channel to prevent data overruns.

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28. The system of claim 25,

wherein the self configuration link is inserted in the first plurality of transfer links;

wherein, the DMA Controller is operable to execute the first plurality of transfer links on a DMA channel; and

wherein when the DMA channel is operable to notify the host to begin transferring the second plurality of transfer links to the second portion of the link buffer when the DMA channel reaches the self configuration link.

29. The system of claim 25,

wherein the self configuration link is inserted in the second plurality of transfer links;

wherein, the DMA Controller is operable to execute the second plurality of transfer links on a DMA channel; and

wherein when the DMA channel is operable to notify the host to begin transferring the third plurality of transfer links to the first portion of the link buffer when the DMA channel reaches the self configuration link.

30. The system of claim 16,

wherein the communication medium comprises an IEEE 1394 bus, which is compliant with an IEEE 1394 protocol specification.

31. The system of claim 16,

wherein the data acquisition device comprises a PCI device,

wherein the data acquisition device further comprises a PCI/1394 translator; and

wherein the PCI/1394 translator is operable to translate messages between the IEEE 1394 protocol and PCI, thereby providing a mechanism for communication between the IEEE 1394 bus and the PCI device.

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